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EXAMINER	
THOMAS, SHANE M	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/685,579	KURAFUJI, TAKASHI	
	Examiner	Art Unit	
	Shane M. Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/16/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is responsive to the application filed 10/16/2003. Claims 1-15 are presented for examination and are currently pending.

The examiner requests, in response to this Office action, any reference(s) known to qualify as prior art under 35 U.S.C. sections 102 or 103 with respect to the invention as defined by the independent and dependent claims. That is, any prior art (including any products for sale) similar to the claimed invention that could reasonably be used in a 102 or 103 rejection. This **request** does not require applicant to perform a search. This request is not intended to interfere with or go beyond that **required** under 37 C.F.R. 1.56 or 1.105.

The request may be fulfilled by asking the attorney(s) of record handling prosecution and the inventor(s)/assignee for references qualifying as prior art. A simple statement that the query has been made and no prior art found is sufficient to fulfill the request. Otherwise, the fee and certification requirements of 37 CFR section 1.97 are waived for those documents submitted in reply to this request. This waiver extends only to those documents within the scope of this request that are included in the application's first complete communication responding to this requirement. Any supplemental replies subsequent to the first communication responding to this request and any information disclosures beyond the scope of this are subject to the fee and certification requirements of 37 CFR section 1.97.

In the event prior art documentation is submitted, a discussion of relevant passages, figs. etc. with respect to the claims is requested. The examiner is looking for

specific references to 102/103 prior art that identify independent and dependent claim limitations. Since applicant is most knowledgeable of the present invention and submitted art, his/her discussion of the reference(s) with respect to the instant claims is essential. **A response to this inquiry is greatly appreciated.**

The examiner also requests, in response to this Office action, that support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line no(s). in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

Excerpts from all prior art references cited in this Office action shall use the shorthand notation of (column # / lines A-B) to denote the location of a specific citation. For example, a citation present on column 2, lines 1-6, of a reference shall herein be denoted as "(2/1-6)."

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d) on 10/16/2003, which papers have been placed of record in the file.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 10/16/2003 was considered by the examiner. A signed copy has been enclosed herewith.

Specification

The Examiner recommends amending the term --peculiar-- to a more widely recognized term in the art such as --unique-- so as to clarify the specification language.

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

Claims 3-6,9,10, and 13-15 are objected to because of the following informalities:

As per claim 3, the Examiner recommends amending line 5 to read: "said power control circuit only supplying [[a]] power to the ~~only~~ one or more cache" in order to clarify the wording of the claim limitation.

As per claims 4- 6,9,10,13, and 14, the Examiner recommends amending lines 7 (claims 4,5,10,13, and 14) and line 8 (claim 10) to read: "said tag memory stores said tag [[in]] of said cache address" and lines 6-7 (claim 6) to read: "... tag memories for storing said tag [[in]] of said cache address, and ..." in order to properly clarify that the tag portion of the cache address is being stored and *not* that the tag is *being stored in* the cache address.

Further regarding claim 6, the Examiner recommends amending the term --peculiar-- to a more widely recognized term in the art such as --unique-- so as to clarify the claim language. The Examiner shall interpret the limitation of --peculiar-- to mean --unique--.

As per claim 15, the Examiner recommends amending the term --bank control signal-- of lines 10-11 and 12 to --bank select signal-- in order to maintain coherence throughout the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 8-14 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 8-14 set forth a method for designing a cache; however, the claim, as required by MPEP ¶2106, needs to be a practical application of the cache design idea and not the idea itself. In other words, merely deigning a cache is an abstract idea rather than the practical application of the idea. Such a practical application of the idea can be established through producing a useful, concrete, and tangible result. The steps laid out in claims 8-14 appear to produce a useful result, but do not however, create a tangible result. In the method claimed in the limitations of claims 8-14 does not execute a step that would result in a tangible result (i.e. conveying the design to a user through display, printing or transmission of the cache design, storing the cache design for later retrieval, etc.). Furthermore, Applicant's specification, specifically, ¶¶247-289, does not describe or teach such a tangible step.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 8-14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention for the reasons set forth in the 35 U.S.C. 101 rejection discussed supra. Specifically, neither the claims nor specification as originally filed, teach how the method of cache design can produce a useful, concrete, and tangible result.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-7, 9, and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 1 and 3, it is not clear whether the term --said signal-- refers to the --at least one control signal selected out of the plurality of control signals-- or the --signal indicative of cache capacity-- as the term --said signal-- lacks antecedent basis. Nonetheless, for the purposes of examination, the Examiner has interpreted --said signal--

to be the --signal indicative of cache capacity--. The Examiner recommends labeling the --signal indicative of cache capacity-- as a --cache capacity signal--, or the like, to overcome this rejection.

As per claims 9 and 10, it is not clear whether the term --said cache memory device-- (line 2) is referring to the --a cache memory device-- of line 1 (which in itself is ambiguous since more than one cache memory device is being claimed as being designed in base claim 8), the --first cache memory device-- of claim 8, or the --second cache memory device--, as the term --said cache memory device-- lacks antecedent basis. Nonetheless, for the purposes of examination, the Examiner shall interpret the term --said cache memory device-- to be the second cache memory device, where the second cache memory device comprises two cache memories as discussed below.

Claims 2 and 4-6 are dependent upon rejected claim 1.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,2,4-7, and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Chin et al. (U.S. Patent No. 6,678,018). Further, the prior art reference of Ghosh et al. (U.S. Patent Application Publication No. 2002/0069333) is used for inherent teachings not disclosed or taught by Chin et al.

As per claim 1, Chin teaches [**at least one cache memory**] (214 and 216 of figure 2) ands [**storing copy data of a main memory**] (i.e. RAM memory) in (2/23-33). Further Chin teaches [**a bank control circuit**] (motherboard 200) [**connected to said at least one cache memory**] (installed on the motherboard - abstract and figure 2) [**and capable of generating a plurality of control signals for access**] (signals 228 and 226 are set for master/slave control of accesses between the cache memories 214 and 216 and also a third control signal - result of address bit 21, which determines which cache data is to be accessed - (3/9-31)). [**The bank control circuit**] 200 [**receives a signal indicative of cache capacity**] inherently from the connectors 210 and 212 so the bank control circuit can distinguish whether or not one or two cache memories are installed on the bank control circuit (2/34-36) and (3/7-15). [**One control signal**] (signal of address bit 21) [**selected from the plurality of control signals**] (signals 228,226, and the signal of address bit 21) is used to [**access said at least one cache memory, respectively in**

accordance with said (cache capacity) signal] as taught in (3/7-31). Chin teaches accessing the data portion of the cache on card 214 or 216 when the control signal of address bit 21 is '0' or '1', respectively.

As per claim 2, the **[bank control circuit controls access to said at least one cache memory in such a manner that one accessing operation implements access to only one out of said at least one cache memory]** as taught in (3/11-14) where, depending on the control signal of address bit 21, only one of the caches on cards 214 and 216 are accessed.

As per claim 4, Chin teaches in figure 3 and (2/45-59) a **[cache address]** bits 3-29 **[indicating an address of main memory]** bits 0-31 **[and including a tag]** bits 29-22 **[and an index]** bits 5-20 **[is input to said cache memory device]** (figure 1, 116). **[A bit position occupied by said tag and index is fixed in said cache address]** is taught by Chin since the bit position of the tag and index do not changed based on the number of L2 caches present in the system (figure 3). The **[at least one cache memory]** of cards 214 and 216 each have a **[tag memory]** 220 and **[sets the index in the cache address to be an address]** by which the tag memory 220 is access - (2/55-57). The **[tag memory stores said tag (of) said cache address]** by storing cache address bits 21-29 in the tag RAM 220 (2/57-59).

Chin teaches a **[cache peripheral circuit]** (figure 2, 218) that **[links the index of the cache address input to the cache memory device when one or more cache memories accessed with at least one control signal selected by the bank control circuit]** (as discussed supra) **[is accessed, to data in the tag memory stored in the address indicated by the index]** as well known in the caching art and shown in figure 3 and taught in (2/52-59). Further, the **[cache peripheral circuit generates and outputs a copy back address]** (via the bi-directional address bus as shown in figure 2) as part of the inherent copy-back (or write-back) scheme that is

employed by the system of figure 1. A copy-back (or write-back as also named in the art) scheme is known in the art to be a method of writing back data from the cache to the main memory. Chin teaches that the system of figure 1 is an arrangement of a Pentium™ microprocessor and Ghosh et al. teaches that Pentium™ caches use a write-back (copy-back) scheme (¶15). Additionally, Chin specifically teaches in (4/4-22) that flushing of the L2 cache may occur as well. The term "flushing" is known in the art to be associated with write-back (copy-back) caching; when a flush occurs, modified data is written from the cache back to main memory. Therefore, since the system of Chin implements a copy-back scheme for updating main memory data, the cache peripheral circuit 218 must therefore generate and output the address of the modified data stored in the data caches of cards 214 and 216 in order to modify the correct locations of main memory (i.e. the copy-back addresses).

Therefore, as discussed above, it can be seen that the system of Chin employs a [**copy back method using the copy back address as a writing method for main memory**].

As per claim 5, the rejection of lines 1-7 follows the rejection for claim 4, lines 1-7, discussed supra. Regarding the remainder of claim 5, Chin teaches in a [**comparator**] 314 [**for comparing the tag in the cache address input to the cache memory device when one or more cache memories accessed with said at least one control signal selected by said bank control circuit**] (as discussed supra) [**is accessed, to data in the tag memory stored in the address indicated by the index in said cache address and for detecting their coincidence/no-coincidence**] - (2/52-64).

As per claim 6, the [**at least one cache memory**] 116 of Chin actually can have a [**plurality of cache memories**] (comprised on cards 214 and 216 as shown in figure 2 and taught in 2/34-44). Chin teaches in figure 3 and (2/45-59) a [**cache address**] bits 3-29 [**indicating an address of main memory**] bits 0-31 [**and including a tag**] bits 29-22 [**and an index**] bits 5-20 [**is input to said cache memory device**] (figure 1, 116). [**A bit**

position occupied by said tag and index is fixed in said cache address] is taught by Chin since the bit position of the tag and index do not changed based on the number of L2 caches present in the system (figure 3).

The [**plurality of cache memories have respective tag memories for storing the tag of the cache address**] as taught in (2/34-44). Chin teaches that the [**respective tag memories**] 220 [**store plural pieces of fixed data peculiar to said plurality of cache memories, respectively**] because each tag RAM 220 of cache 214 or 216 can only store the data corresponding to whether the control signal of the address bit 21 is active, meaning that for cache addresses which have address bit 21 set as '0', the cache RAMs on card 214 will be accessed whereas if the address bit 21 is set as '1', the cache RAMs on card 216 will be accessed - (3/11-14). Thus, it can be seen (figure 3) that depending on the address bit 21 of the incoming address, the plural fixed data pieces (fixed because the number of tag bits never change as discussed supra) are stored in the plurality of tag memories. [**Each of the plural pieces of fixed data**] (i.e. bits 22-29 of the incoming address previously stored in Tag RAM 312) [**correspond to a part of the tag**] since the Tag RAM 312 stores every part of the incoming tag as known in the art and shown in figure 3.

As per claim 7, the [**at least one cache memory**] 116 of Chin actually can have a [**plurality of cache memories**] (comprised on cards 214 and 216 as shown in figure 2 and taught in 2/34-44). The [**plurality of cache memories have the same memory capacity**] since each of the memory cards comprising the cache RAMs of Chin are identical (2/34-44).

As per claim 15, Chin teaches a [**bank control circuit**] 200 [**controlling access to a cache memory**] (combination of the caches on cards 214 and 216) that comprises a [**decoder**] (combination of the logic portion of the controllers 218 of the cards 214 and

216 that is shown in figure 4) [**receiving first and second signals**] (SINGLE signal indicating more than one cache card is installed on the bank control circuit 200 and BIT 21 signal of incoming cache address as shown in figure 4, respectively) [**and outputting bank select signals**] (each controller outputs the signal result of OR gate 412 in order to activate its respective cache - 3/32-50) [**such that one of the bank select signals is active in accordance with said first and second signals**] (as shown in figure 4 and taught in 3/11-50), the bank control signal - result of OR gate 42 - for the "master" card 214 cache is active when the first signal is inactive '0' and the second signal is active '1' and the bank select signal for the "slave" card 216 cache is active when both the first and second signals are inactive '0') [**wherein said first signal is indicative of a cache capacity used in the cache memory**] (SINGLE signal designates whether one or two caches are present in the system of Chin - (3/43/46)) [**and the second signal is a part of an address supplied to the cache memory**] (BIT 21 is the 21st bit of an incoming cache address - (3/7-15)).

Further, Chin teaches [**signal output circuits**] (the portion of the controller 218 that actually sends data to and from the tag ram 220 and data ram 222 via the buses shown on figure 2) [**provided correspondingly to the bank select signals, respectively**] since in order for the signal output circuits to forward information received from the address/control bus 112 and data bus 110, the bank select signal (output of respective OR gate 412) must be active (3/41-50). [**Each signal output circuit receives a control signal for accessing the cache memory**] (one of control signals shown in figure 2 being transmitted between the controllers 218 and the bus 101 or any address signal that could be transmitted to the tag or data RAMs from the bus 110) [**and a corresponding bank**

select signal] (since the output of the OR gate 412 is needed in order to determine whether or not the respective tag and data RAMs will be accessed) **[and permitting the control signal to be output to the cache memory in response to an active state of said corresponding bank select signal]** (data is forwarded to the RAMs when the respective bank select circuit is active - (3/41-50)) **[while inhibiting said control signal to be output to the cache memory in response to a non-active state of said corresponding bank select signal]** (likewise it can be inferred such that when the output of the OR gate 412 is inactive, the corresponding RAMs are not accessed - (3/41/50)).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chin et al. (U.S. Patent No. 5,678,018) in view of Shiell et al. (U.S. Patent No. 6,442,667).

As per claim 3, the **[at least one cache memory]** 116 of Chin actually can have a **[plurality of cache memories]** (comprised on cards 214 and 216 as shown in figure 2 and taught in 2/34-44). Further, Chin teaches that depending on the incoming address bit 21 that only one of the two caches on cards 214 and 216 are accessed (3/11-14). As it is well known in the art that caching components require power to operate, **[a power control circuit]** (i.e. a portion of the motherboard that controls power to the plurality of

caches on cards 214 and 216 - probably via the motherboard connectors 210 and 212 (2/34-36)) **[for controlling power supply to the plurality of cache memories connected to the bank control circuit based on said signal** is an inherent component of the motherboard (bank control circuit) 200 since only the first cache would be supplied power when there is only one cache card 214 installed and when the second or slave card comprising the second L2 cache is installed, and the SINGLE signal inactive, would it be seen that the second cache would have been supplied with power as well, thereby enabling the CPU 120 the ability to access the second L2 cache. However, Chin does not specifically teach the cache memory device of figure 2 further comprising a [**power control circuit supplying power to one or more cache memories accessed with said at least one control signal selected by said bank control circuit out of the plurality of cache memories**]. In other words, Chin does not teach supplying power to only the cache memory 214 or 216 which currently needs to be accessed (i.e. bit 21 of the incoming address) by a cache request.

Shiell teaches a method to only power a portion of an L2 cache memory based on translated (i.e. decoded address bits) (7/21-23) and (9/6-10). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the selective caching system of Chin with the teaching of selectively supplying of power to only the portion of the cache that is currently being accessed of Shiell in order to have gained reduced the overall power dissipation of the combined L2 cache (214, 216). One having ordinary skill in the art would have seen that such a modification to the system of Chin would have yielded immediate benefits. By using translated bits of the incoming address (namely address bit 21), modified Chin would

have been able to not only select which cache was to perform the requested read or write access, but with the teaching of Shiell, would have been able to supply power to only that same cache (214, 216), thereby conserving the power that would have been required to operate the other cache card not being accessed when it would not have been required to have been accessed.

Claims 8-11, 13, and 14, are rejected under 35 U.S.C. 103(a) as being unpatentable over Chin et al. (U.S. Patent No. 5,678,018).

As per claim 8, Chin teaches in (4/30-33) that more than two caches are contemplated and would simply require the use for more than just the address bit 21 for accessing the cards and multiple binary digits to code the cache cards. Thus it would have been seen by one having ordinary skill in the art that if two address bits were used to access the more than two cache cards anticipated by Chin, that four caches could have been used (signified by "00," "01," "10," and "11" of the two address bits). Therefore Chin teaches [**designing a bank control circuit**] (motherboard 200) [**that is connectable to a first predetermined number of plural cache memories**] (such as four cache memories similar to cache memories on cards 214 and 216 of figure 2) and [**capable of permitting one or more cache memories of the first predetermined number of plural cache memories to be accessed**] (based on the decoding of the two address bits required to select which of the four caches is to be accessed by a current cache request) and [**changing the number of the one or more cache memories to be permitted to be accessed**] since, invariably, the SINGLE line of figure 4 and (3/11/14) would have been two bits as well to indicate how many cache cards like 214 and 216 are connected to the

bank control circuit 200. Since any number between 1 and 4 cache cards could be installed in a system with four cache slots as anticipated by Chin (4/30-33), the bank control circuit 200 would change the number of said one or more cache memories permitted to be accessed by control of the activation of the SINGLE lines, which would have indicated the number of caches currently attached to the system - (3/41-50).

For simplicity purposes, the Examiner is considering the bank control circuit to be the motherboard 200 as previously discussed above while considering a --cache memory device-- to be a device that comprises the caches as well as the bank control circuit, such as the --device-- as shown in whole figure 1 of Chin.

Chin teaches [**designing a first cache memory device including a bank control circuit designed in step (a)**] (system of figure 1 - as taught directly above - in 2/34-3/50).

Chin does not specifically teach [**designing a second cache memory device**] (aside from the first one taught in figure 2 and (2/34-3/50) with modification as suggested by motivation found on (4/30-33)) [**including a bank control circuit designed in step (a)**] (which the Examiner is interpreting as being in addition to the first cache memory device as discussed directly above with the four cache cards); however, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have designed a second cache memory that included the same bank control circuit (motherboard 200) as the first cache memory device as taught and discussed herein by Chin, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art (refer to MPEP § 2144.04).

Further, the Examiner is interpreting the step of **[(b-1) designing a second predetermined number of cache memories which is equal to or smaller than said first predetermined number]** to be the four cache memories (discussed above) that are used in the system of Chin when the bank control circuit (designed in step (a)) is part of the system of figure 1 - the first cache memory device. As could have been seen with this interpretation, the second predetermined number of cache memories is equal to (four) the first predetermined number, with the only difference being that the second predetermined number are part of the first cache control circuit as shown in figure 1 and not just a part of the stand alone bank control circuit (not comprised in a cache memory device).

Finally, Chin teaches by way of (4/30-33) and using the same logic above with regard to using two bits of address to determine which cache card to access for the present cache request, that **[a third predetermined number of cache memories which is equal to or smaller than the first predetermined number and is different from said second predetermined number]** (with four cache cards) could be designed as originally suggest by Chin in (2/23-3/50), where only two cache memories, instead of four like in the first cache memory device, are utilized. It would have been obvious to one having ordinary skill in the are to have designed the second cache memory device to only use one bit of address to determine which cache to access and only one (i.e. the SINGLE signal) line to determine the number of caches connected to the second memory device. Further, it can be seen that the third predetermined number (two) is smaller than the first predetermined number (four) and different from the second predetermined number (four).

As per claim 9, the rejection of lines 1-15 follow the rejection for claim 4, discussed supra, with a [**cache peripheral circuit**] being [**designed**] as shown in figure 2, element 218, with a portion of the design logic shown in figure 4. Chin does not specifically teach the [**first and second cache memory devices further comprising the cache peripheral circuit in step (d) are designed at steps (b) and (c), respectively**], but it would have been obvious to one having ordinary skill to have designed the cache peripheral circuit in steps (b) and (c) since these steps actually create the cache circuits themselves and the cache peripheral circuit is being interpreted as the logic required to access the cache memories. Further since there are two cache memory devices and since Chin teaches a single cache memory device comprising a cache peripheral circuit 218, it would have further been obvious to one having ordinary skill in the art at the time the invention was made to have designed a cache peripheral circuit for each cache memory device that was being created in order to have utilized the cache peripheral circuit in order to access the cache (i.e. a cache controller), as well known in the caching art.

As per claim 10, the rejection of lines 1-12 follows the rejection for claim 5, discussed supra, with [**a comparator**] being [**designed**] in figure 3, element 314, and (2/52-64). Chin does not specifically teach the [**first and second cache memory devices further comprising the comparator in step (e) are designed at steps (b) and (c), respectively**], but it would have been obvious to one having ordinary skill to have designed the comparator in steps (b) and (c) since these steps actually create the cache circuits themselves and the comparator is being interpreted as the logic required to determine whether or not requested cache data is present in the cache. Further since there are two cache memory devices and since Chin teaches a single cache memory device

comprising a comparator 314, it would have further been obvious to one having ordinary skill in the art at the time the invention was made to have designed a comparator for each cache memory device that was being created in order to have utilized the comparator to determine whether or not requested data resides in a cache memory, as well known in the caching art.

As per claim 11, the rejection of lines 1-13 follows the rejection of claim 8, lines 4-13 with one minor exception. With regard to claim 11, the Examiner is considering the first cache memory device comprising the two cache cards 214 and 216 (as discussed in claim 8 as being part of the second cache memory device) and the second cache memory device of claim 11 comprising the four cache caches (as suggested by Chin in 4/30-33).

It would have been obvious by one having ordinary skill in the art at the time the invention was made to have seen that [**redesigning the bank control circuit designed in step (a)**] (i.e. the bank control circuit for the first cache memory device) [**in such a manner that said second predetermined number of cache memories are connected when said second predetermined number is greater than said first predetermined number**] would have been required when expanding the first cache memory device from two cache cards 214, 216 to four cache cards. Such redesign elements would have been seen to include the number of cache card sockets, more than one buddy line, multiple numbers to code the cards, etc (4/30-33).

As per claim 13, the rejection follows the rejection of claim 9.

As per claim 14, the rejection follows the rejection of claim 10.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Arimilli et al. (U.S. Patent No. 6,970,976) teaches that MESI caching coherency protocols are commonly used in combination with write-back (copy-back) caches - (4/37-51).

Guy et al. (U.S. Patent No. 5,282,272) teaches write-back (copy-back) MESI caches holding a distinct advantage over write-through caches - the ability to avoid of bus transactions when writing modified data back to memory each time a cache line is modified, thereby increasing bus bandwidth - (26/39-53).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M Thomas whose telephone number is (571) 272-4188. The examiner can normally be reached M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M Kim can be reached at (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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HONG CHONG KIM
PRIMARY EXAMINER